PhD Aerospace Engineering Doctoral Meeting 2025

Hardware-in-the-Loop for Active Flow Control in Aerodynamics

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CONTEXT & MOTIVATION

Making Planes Smarter — In Real Time

- Traditional flight control uses microcontrollers, but they lack real-time speed.
- Active flow control needs fast, adaptive, low-latency response.
- FPGAs offer deterministic, parallel control at hardware speed.
- A Hardware-in-the-Loop (HIL) setup links CFD and FPGA in real time.
- Reinforcement learning runs on the FPGA to optimize control dynamically.
- Enables smarter, faster, and more efficient aerodynamic control.

Real-Time Flow Control on Reconfigurable Hardware

- FPGAs execute logic in parallel with deterministic timing. Use s programmable logic cells (Figure 1)
- Ideal for real-time control of dynamic aerodynamic systems.
- Used in a Hardware-in-the-Loop (HIL) setup with CFD simulation.
- Enables fast, hardware-level testing of control strategies.

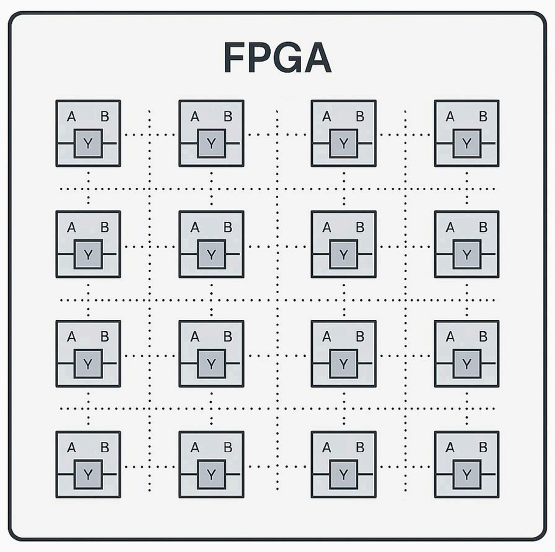


Figure 1. Logic cells in a FPGA

STATE OF THE ART

- Reinforcement learning + FPGAs is gaining traction for real-time flow control [2].
- A recent FPGA-based deep RL system reached 1–10 kHz control rates in supersonic flow [1].
- Outperformed CPU-based systems by 2× orders of magnitude.
- Shows the potential of hardware-accelerated learning in aerodynamics.

SYSTEM ARCHITECTURE OVERVIEW

System Blocks

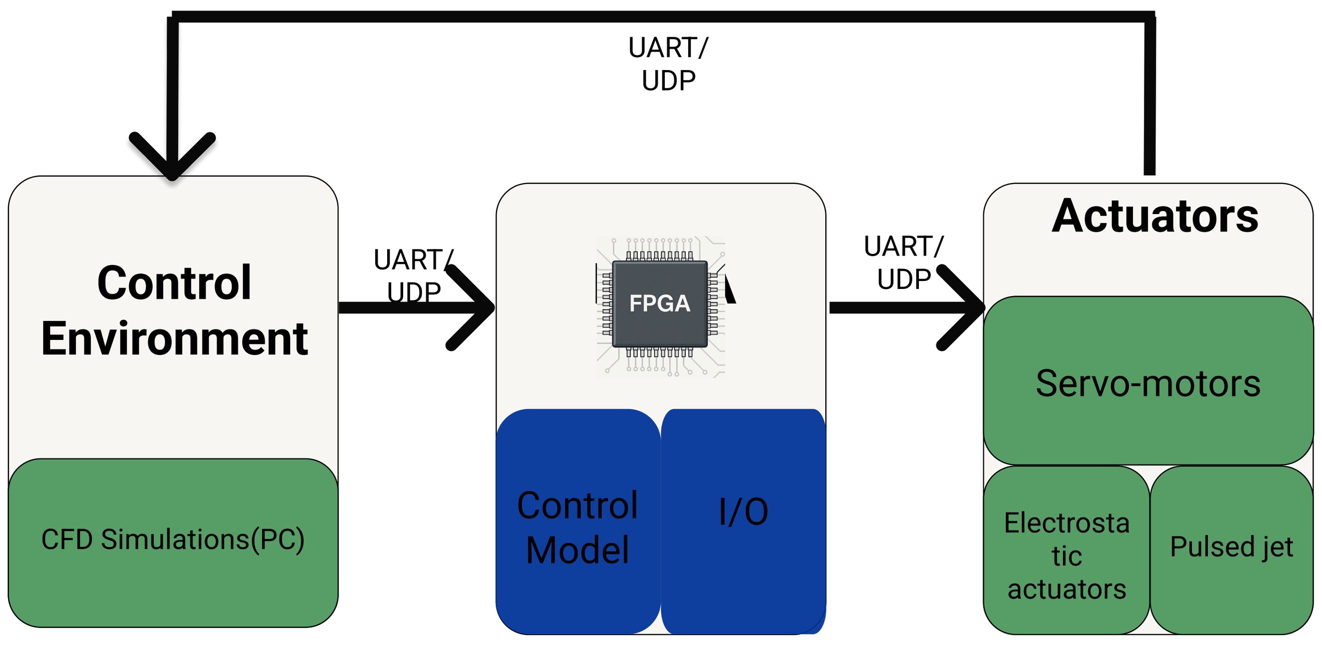
- **Control Model**
  An adaptive controller runs on the FPGA, learning how to respond to changes in the system in real time.
- **Simulation Environment**
  A software-based aerodynamic model mimics realistic flow behavior and feeds sensor-like data to the controller.
- **Hardware Platform**
  A reconfigurable FPGA processes inputs and updates control actions instantly, forming a closed loop between simulation and hardware.

System Diagram

- CFD simulation generates real-time flow dynamics.
- FPGA runs a reinforcement learning controller in hardware.
- UART/UDP link enables low-latency data exchange.
- FPGA receives simulated sensor input (e.g., pressure).
- Control signals update CFD-modeled actuators in real time.
- Forms a closed-loop, hardware-in-the-loop (HIL) setup.
- Enables real-time learning and validation of adaptive control.
- Bridges simulation and physical logic for future deployment.

Reinforced Learning as the control solution

- RL enables adaptive control in nonlinear, dynamic systems.
- Both training and inference run directly on the FPGA.
- Fast updates from real-time sensor feedback.
- Combines learning flexibility with FPGA determinism.
- Ideal for low-latency, continuously improving control.



CURRENT IMPLEMENTATION - PROOF OF CONCEPT

Platform & Design Approach

- Built on Zynq-7000 SoC: FPGA + ARM cores.
- Control logic written in pure Verilog.
- No vendor IP cores — full transparency and portability.

Proof of Concept: Landau Oscillator

- Landau oscillator simulates simplified flow instability.
- Runs on host PC, communicates with FPGA via UART.
- FPGA computes real-time control actions in a feedback loop.
- Validates closed-loop performance under dynamic conditions.
- See Figure 2 for system block diagram.

Early Results

- FPGA successfully:
  - Receives simulated sensor data
  - Runs real-time control logic
  - Closes the loop with a nonlinear system
- Shows that real-time learning and actuation are feasible.
- Still a work in progress, but results are promising.
- Prepares the ground for future CFD integration.

Toolchain & Workflow

- Verification done with cocotb (Python-based testbench).
- Enables fast iteration and high-level control testing.
- Data exchanged via UART using Q16.16 fixed-point format.
- Maintains precision during real-time operation.

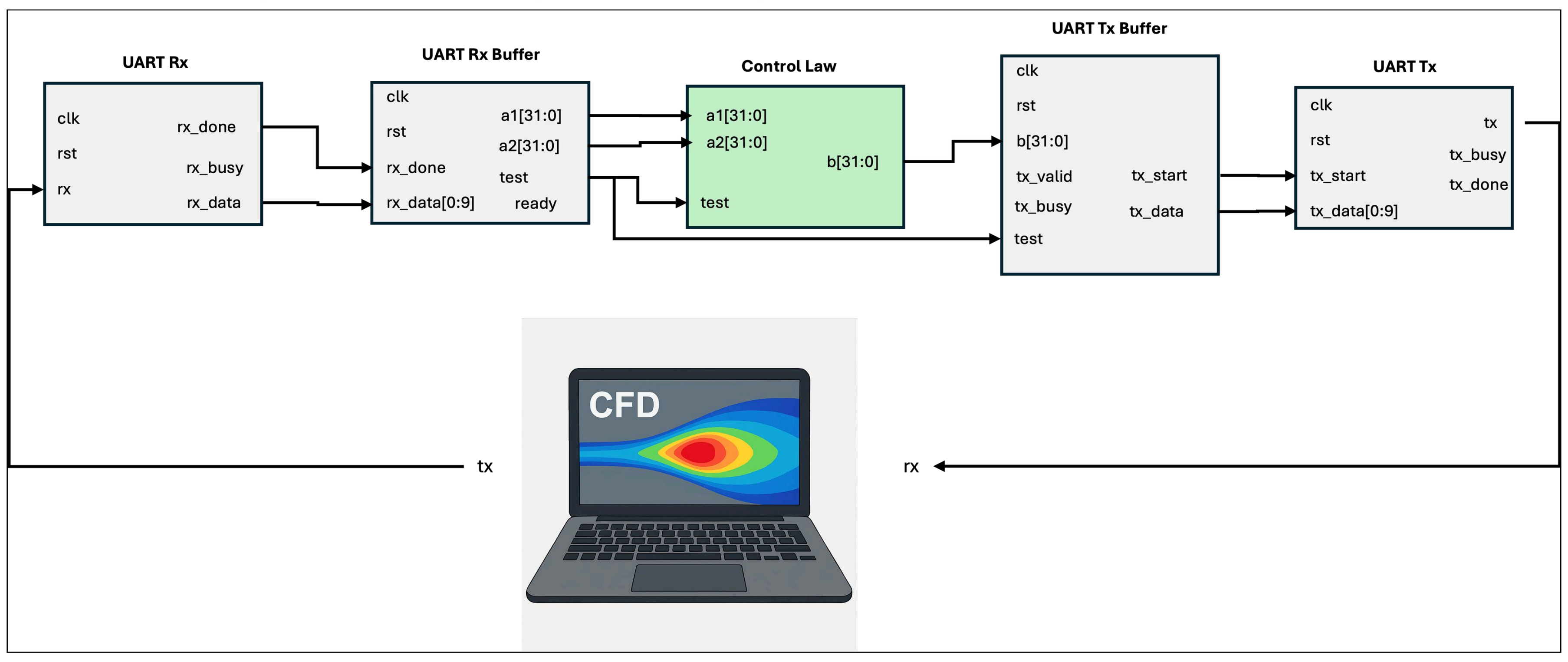


Figure 2. Landau oscillator HIL block diagram

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- [1] Zong H et al. "Closed-loop supersonic flow control with a high-speed experimental deep reinforcement learning framework" JOF 2025
- [2] Jie Chen et al. "Closed-loop plasma flow control of a turbulent cylinder wake flow using machine learning at Reynolds number of 28 000" POF 2024

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